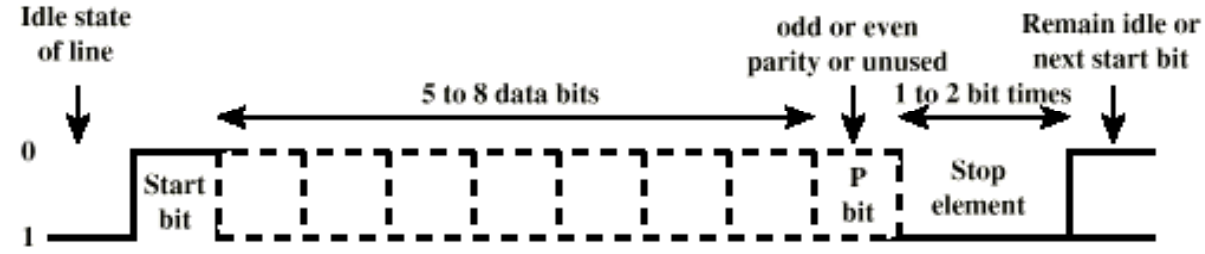
Asynchronous and Synchronous Transmission

- Timing problems require a mechanism to synchronize the transmitter and receiver
- Two solutions
  - —Asynchronous
  - —Synchronous

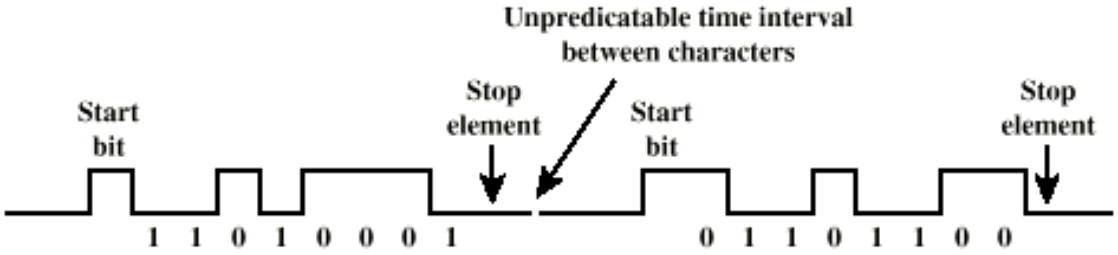
Asynchronous

- Data transmitted on character at a time
  - 5 to 8 bits
- Timing only needs maintaining within each character
- Resynchronize with each character

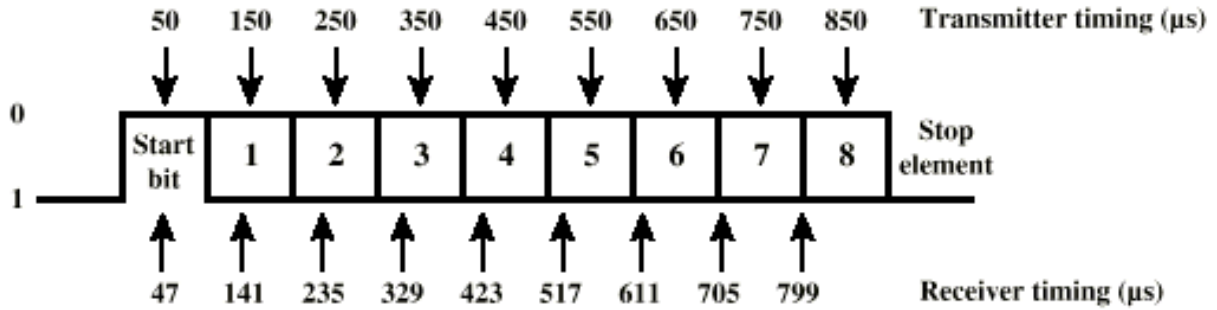
Asynchronous (diagram)



(a) Character format



(b) 8-bit asynchronous character stream



(c) Effect of timing error

Asynchronous - Behavior

- In a steady stream, interval between characters is uniform (length of stop element)
- In idle state, receiver looks for transition 1 to 0
- Then samples next seven intervals (char length)
- Then looks for next 1 to 0 for next char

- Simple
- Cheap
- Overhead of 2 or 3 bits per char (~20%)
- Good for data with large gaps (keyboard)

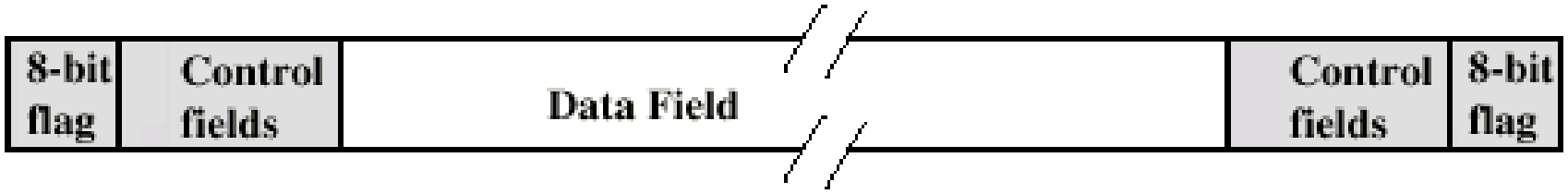
Synchronous - Bit Level

- Block of data transmitted without start or stop bits
- Clocks must be synchronized
- Can use separate clock line
  - —Good over short distances
  - —Subject to impairments
- Embed clock signal in data
  - —Manchester encoding
  - —Carrier frequency (analog)

Synchronous - Block Level

- Need to indicate start and end of block
- Use preamble and postamble
  - e.g. series of SYN (hex 16) characters
  - e.g. block of 11111111 patterns ending in 11111110
- More efficient (lower overhead) than async

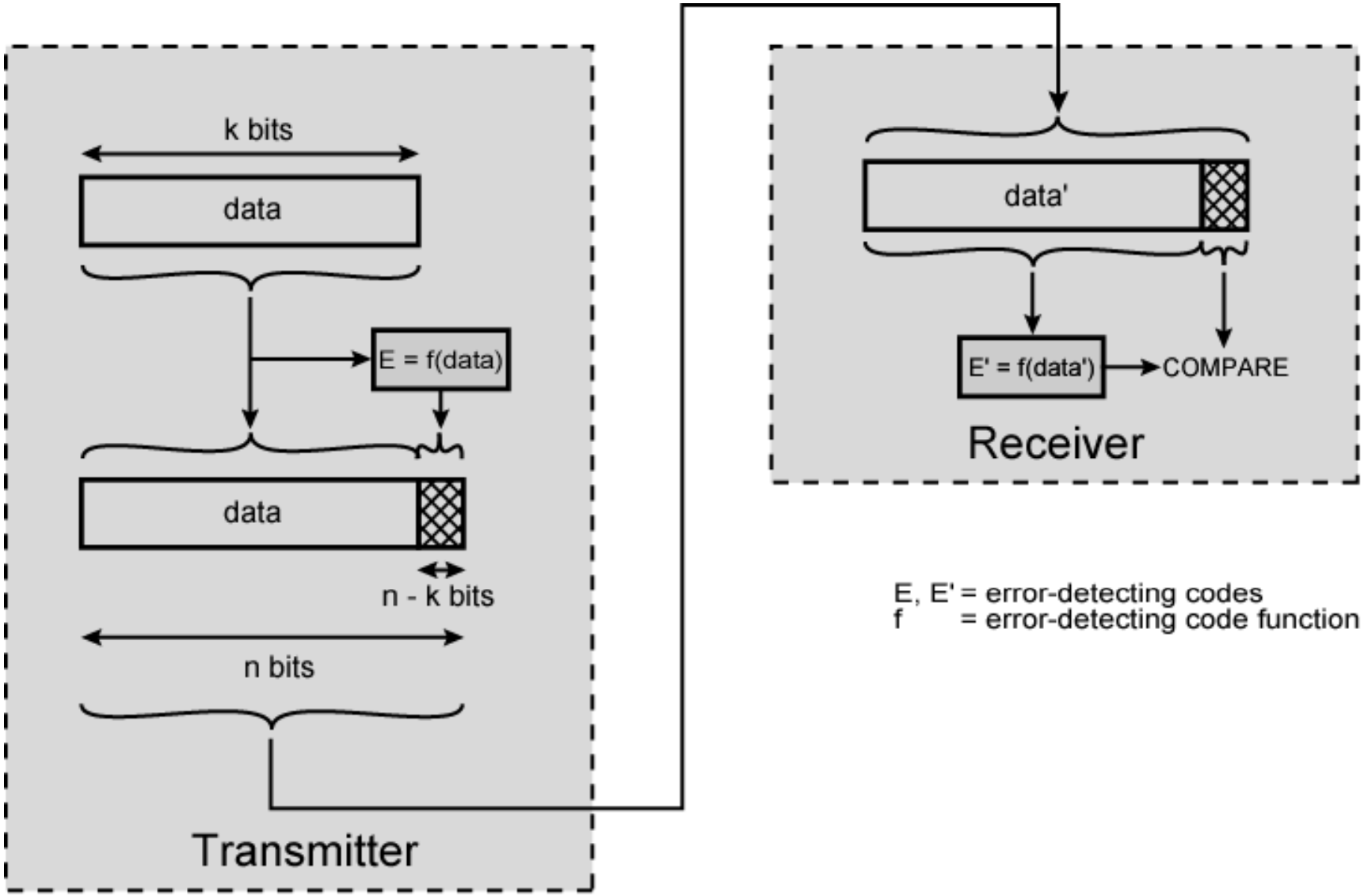
Synchronous (diagram)



Types of Error

- An error occurs when a bit is altered between transmission and reception
- Single bit errors
  - One bit altered
  - Adjacent bits not affected
  - White noise
- Burst errors
  - Length *B*
  - Contiguous sequence of *B* bits in which first last and any number of intermediate bits in error
  - Impulse noise
  - Fading in wireless
  - Effect greater at higher data rates

Error Detection Process



E, E' = error-detecting codes
f = error-detecting code function

Error Detection

- Additional bits added by transmitter for error detection code
- Parity
  - Value of parity bit is such that character has even (even parity) or odd (odd parity) number of ones
  - Even number of bit errors goes undetected

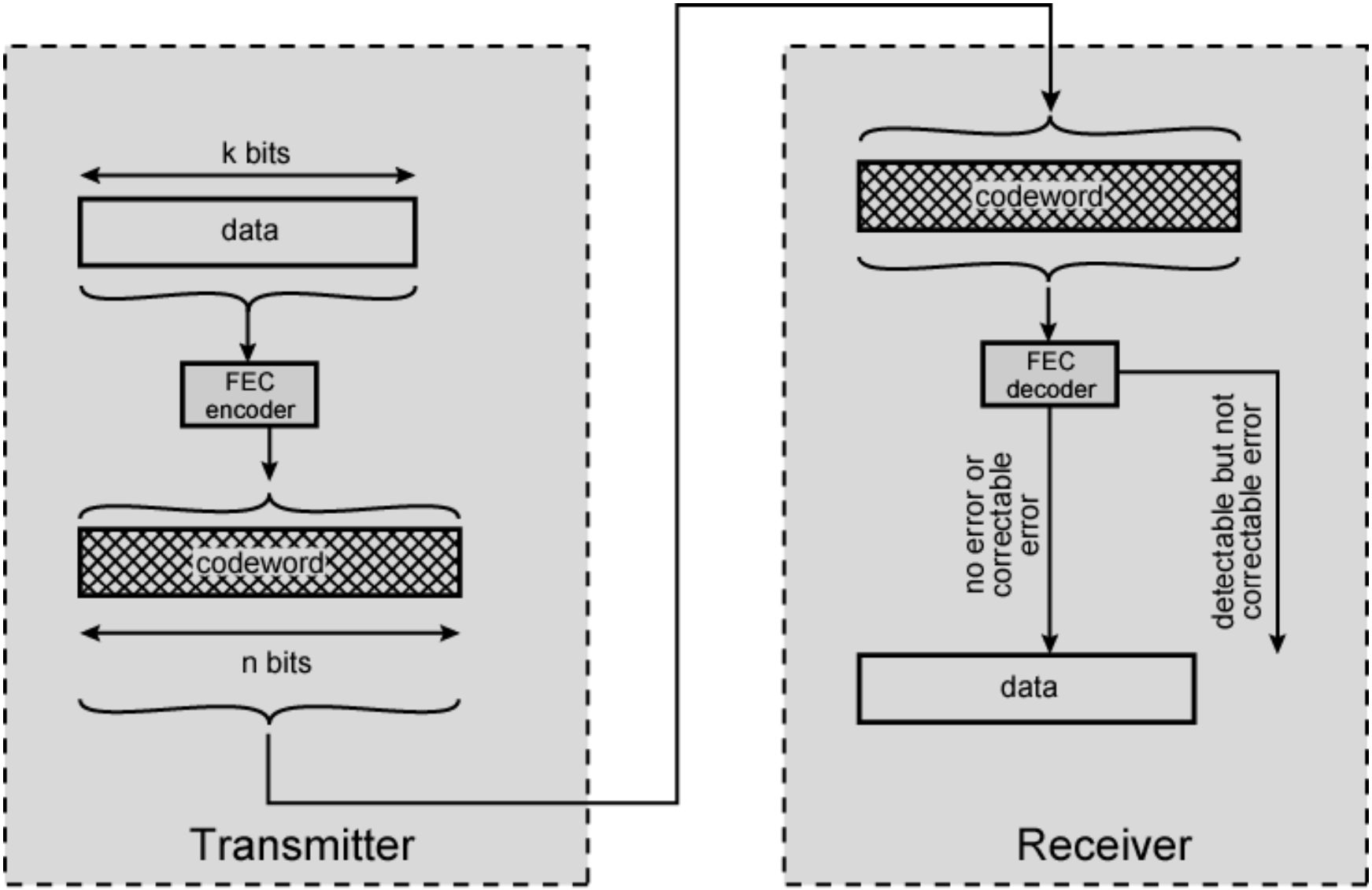
Cyclic Redundancy Check

- For a block of *k* bits transmitter generates *n* bit sequence
- Transmit *k+n* bits which is exactly divisible by some number
- Receive divides frame by that number
  - If no remainder, assume no error
  - For math, see Stallings chapter 6

Error Correction

- Correction of detected errors usually requires data block to be retransmitted (see chapter 7)
- Not appropriate for wireless applications
  - —Bit error rate is high
    - Lots of retransmissions
  - —Propagation delay can be long (satellite) compared with frame transmission time
    - Would result in retransmission of frame in error plus many subsequent frames
- Need to correct errors on basis of bits received

Error Correction Process Diagram



Error Correction Process

- Each *k* bit block mapped to an *n* bit block (*n*>*k*)
  - Codeword
  - Forward error correction (FEC) encoder
- Codeword sent
- Received bit string similar to transmitted but may contain errors
- Received code word passed to FEC decoder
  - If no errors, original data block output
  - Some error patterns can be detected and corrected
  - Some error patterns can be detected but not corrected
  - Some (rare) error patterns are not detected
    - Results in incorrect data output from FEC

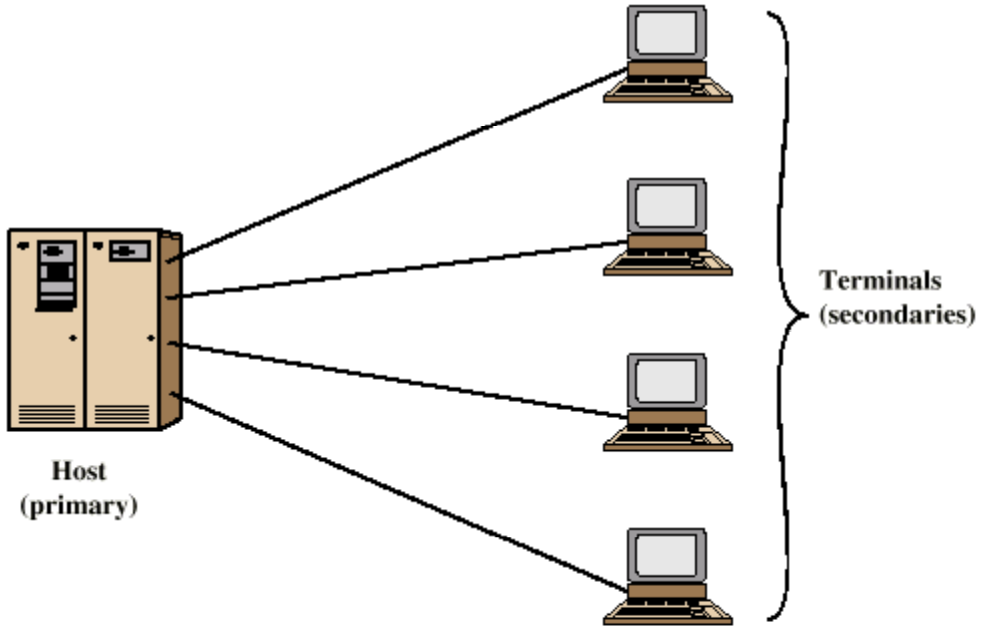
Working of Error Correction

- Add redundancy to transmitted message
- Can deduce original in face of certain level of error rate
- E.g. block error correction code
  - —In general, add ($n - k$) bits to end of block
    - Gives n bit block (codeword)
    - All of original k bits included in codeword
  - —Some FEC map k bit input onto n bit codeword such that original k bits do not appear
- Again, for math, see chapter 6

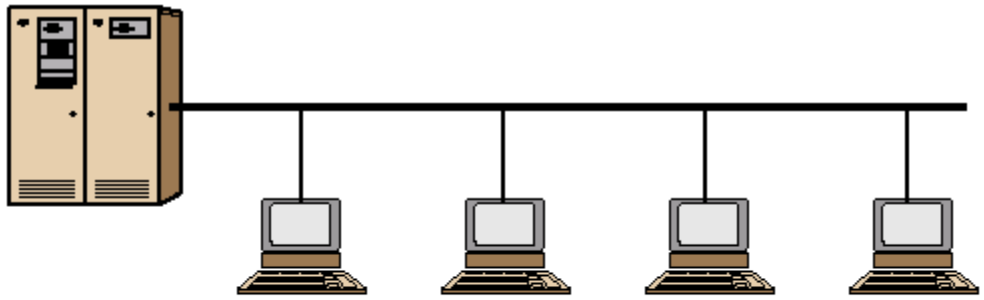
Line Configuration

- Topology
  - Physical arrangement of stations on medium
  - Point to point
  - Multi point
    - Computer and terminals, local area network
- Half duplex
  - Only one station may transmit at a time
  - Requires one data path
- Full duplex
  - Simultaneous transmission and reception between two stations
  - Requires two data paths (or echo canceling)

Traditional Configurations



(a) Point-to-point

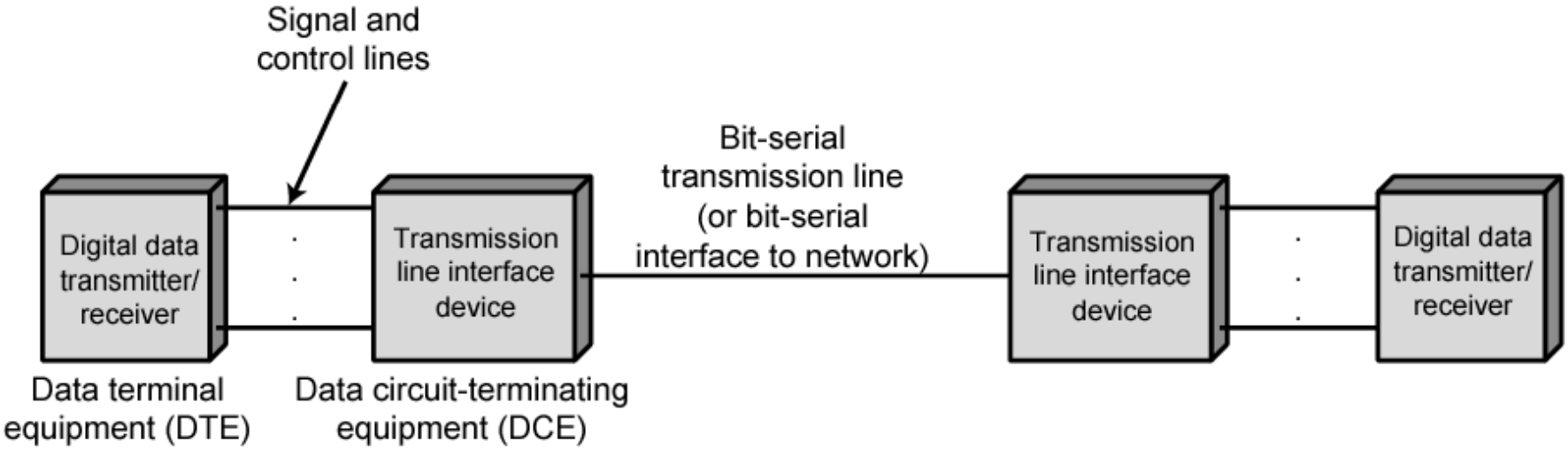


(b) Multipoint

Interfacing

- Data processing devices (or data terminal equipment, DTE) do not (usually) include data transmission facilities
- Need an interface called data circuit terminating equipment (DCE)
  - e.g. modem, NIC
- DCE transmits bits on medium
- DCE communicates data and control info with DTE
  - Done over interchange circuits
  - Clear interface standards required

Data Communications Interfacing



(a) Generic interface to transmission medium

(b) Typical configuration

Characteristics of Interface

- Mechanical
  - —Connection plugs
- Electrical
  - —Voltage, timing, encoding
- Functional
  - —Data, control, timing, grounding
- Procedural
  - —Sequence of events

V.24/EIA-232-F

- ITU-T v.24
- Only specifies functional and procedural
  - References other standards for electrical and mechanical
- EIA-232-F (USA)
  - RS-232
  - Mechanical ISO 2110
  - Electrical v.28
  - Functional v.24
  - Procedural v.24

Mechanical Specification

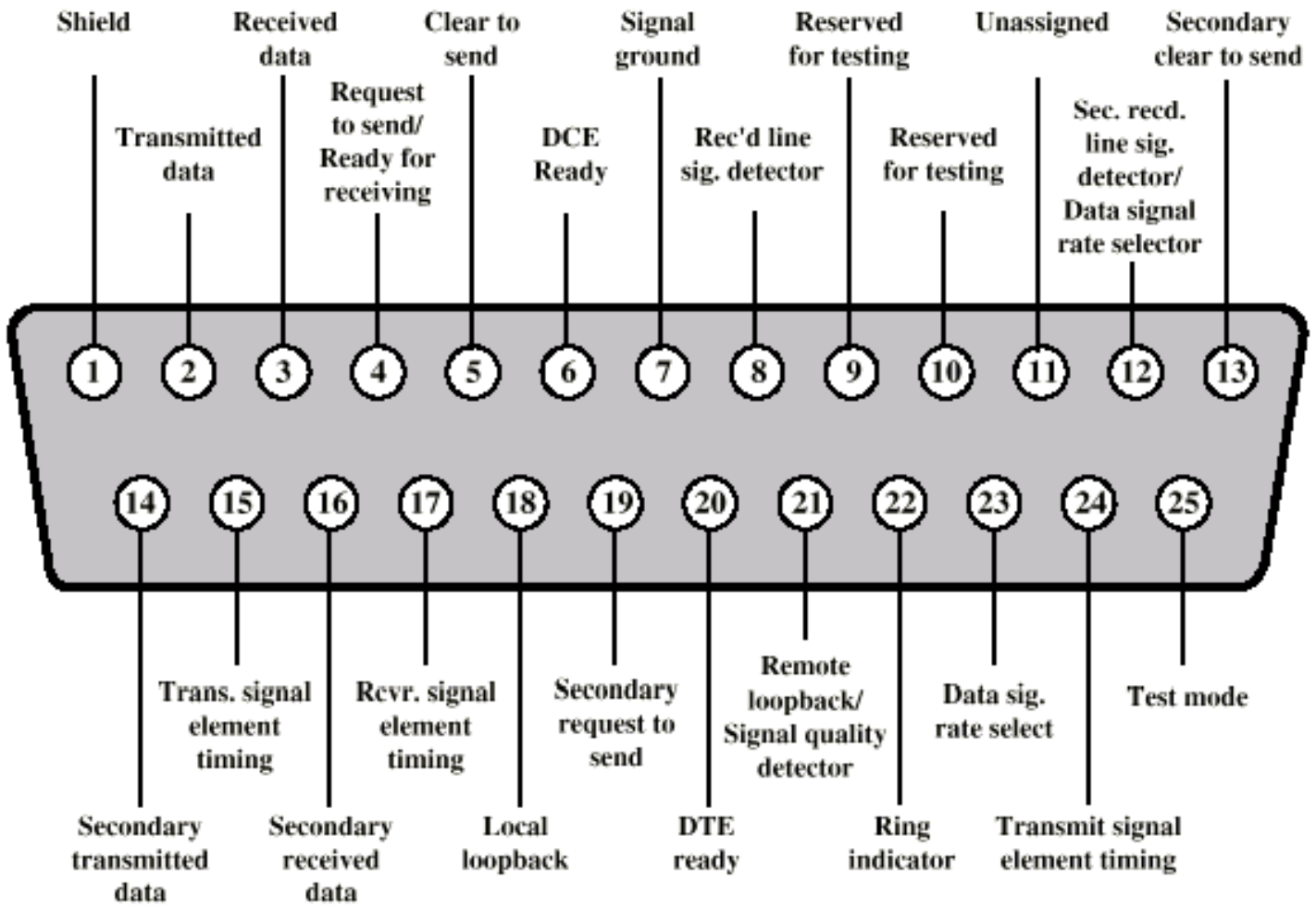


Figure 6.5 Pin Assignments for V.24/EIA-232 (DTE Connector Face)

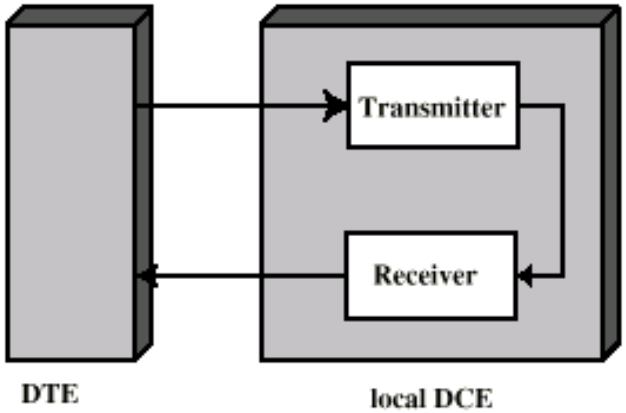
Electrical Specification

- Digital signals
- Values interpreted as data or control, depending on circuit
- More than -3v is binary 1, more than +3v is binary 0 (NRZ-L)
- Signal rate < 20kbps
- Distance <15m
- For control, more than-3v is off, +3v is on

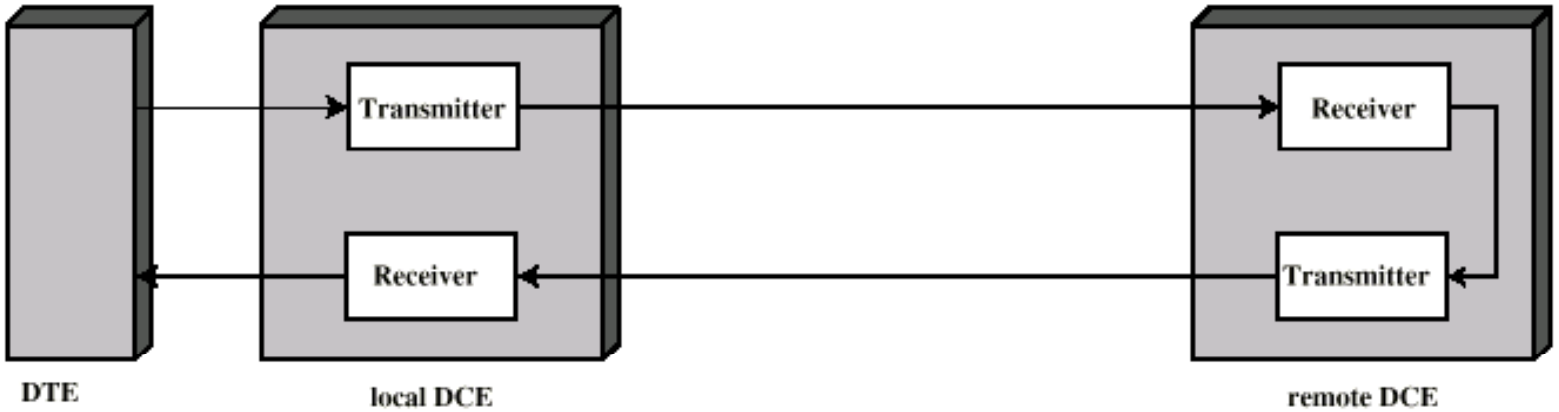
Functional Specification

- Circuits grouped in categories
  - Data
  - Control
  - Timing
  - Ground
- One circuit in each direction
  - Full duplex
- Two secondary data circuits
  - Allow halt or flow control in half duplex operation
- (See table in Stallings chapter 6)

Local and Remote Loopback



(a) Local loopback Testing

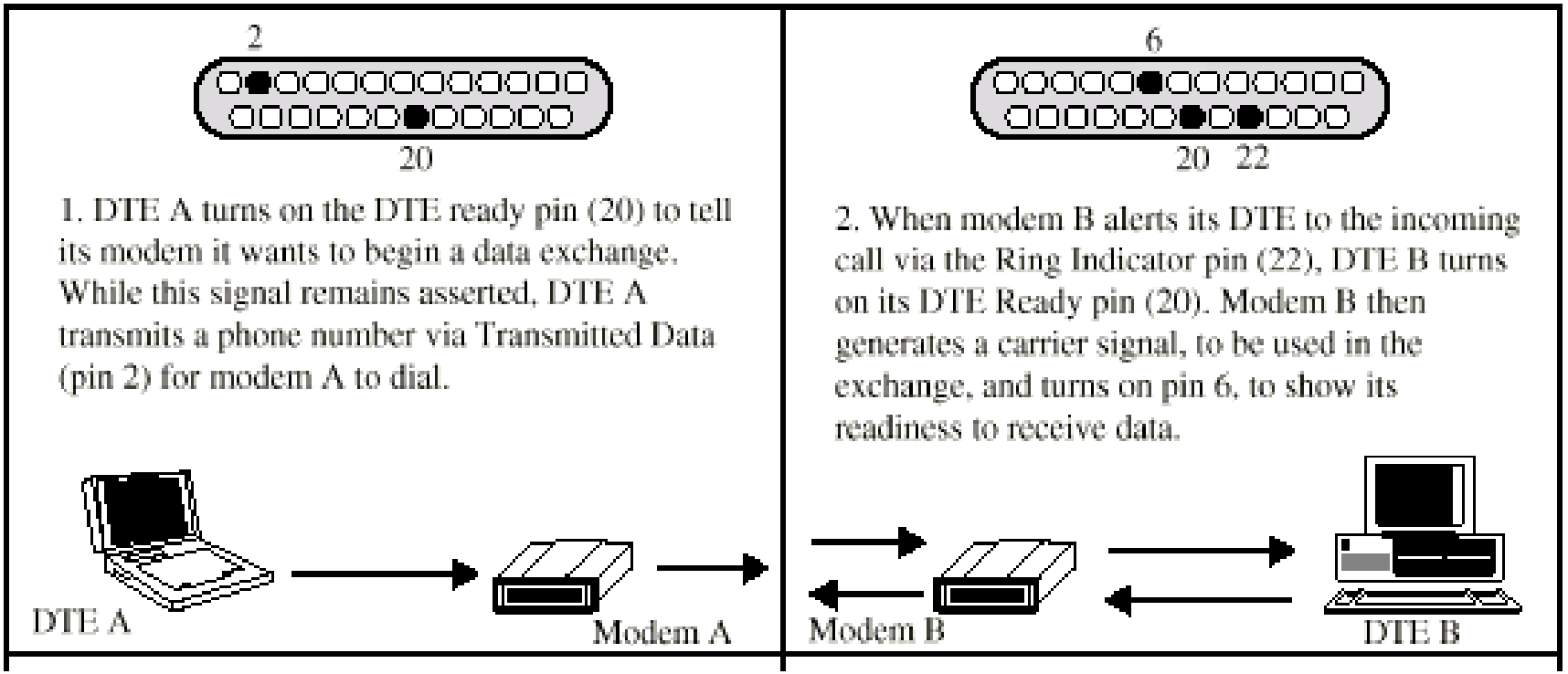


(b) Remote loopback Testing

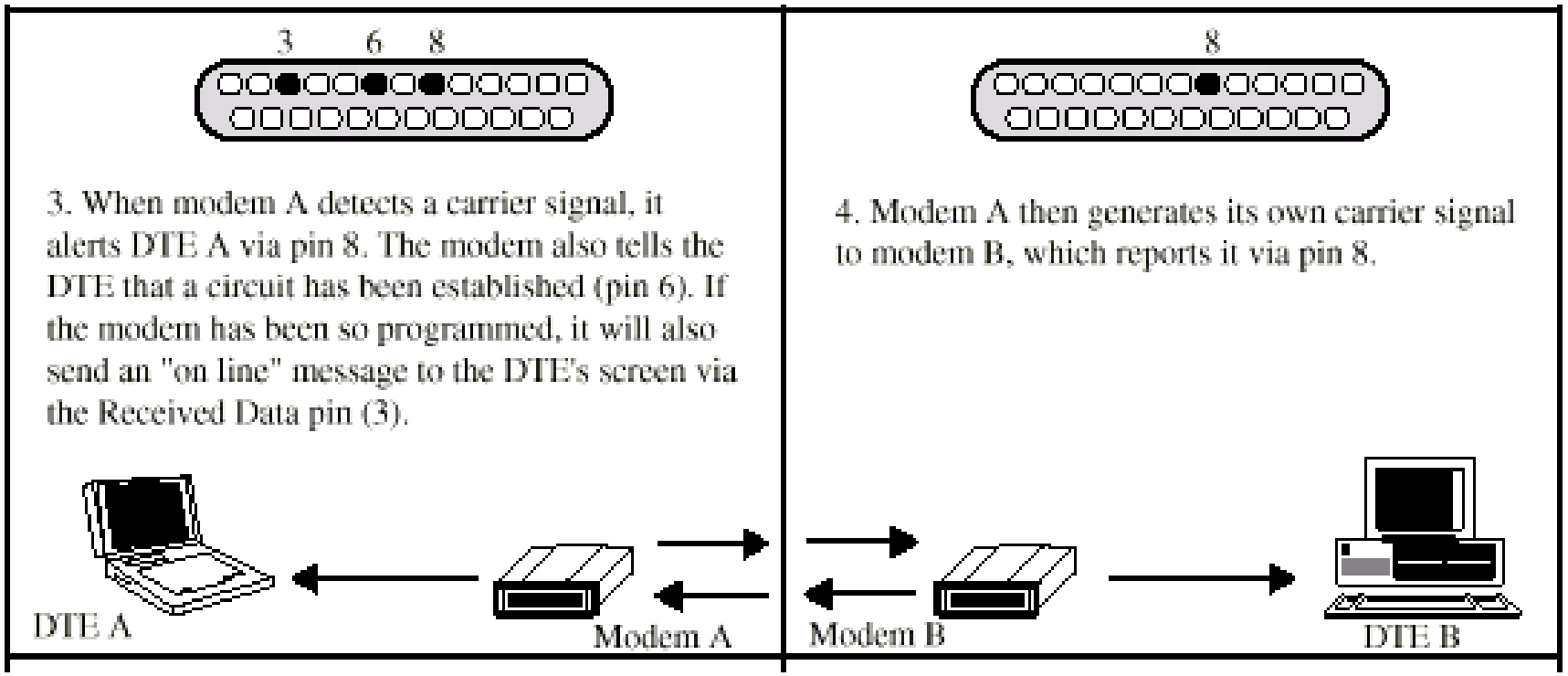
Procedural Specification

- E.g. Asynchronous private line modem
- When turned on and ready, modem (DCE) asserts DCE ready
- When DTE ready to send data, it asserts Request to Send
  - Also inhibits receive mode in half duplex
- Modem responds when ready by asserting Clear to send
- DTE sends data
- When data arrives, local modem asserts Receive Line Signal Detector and delivers data

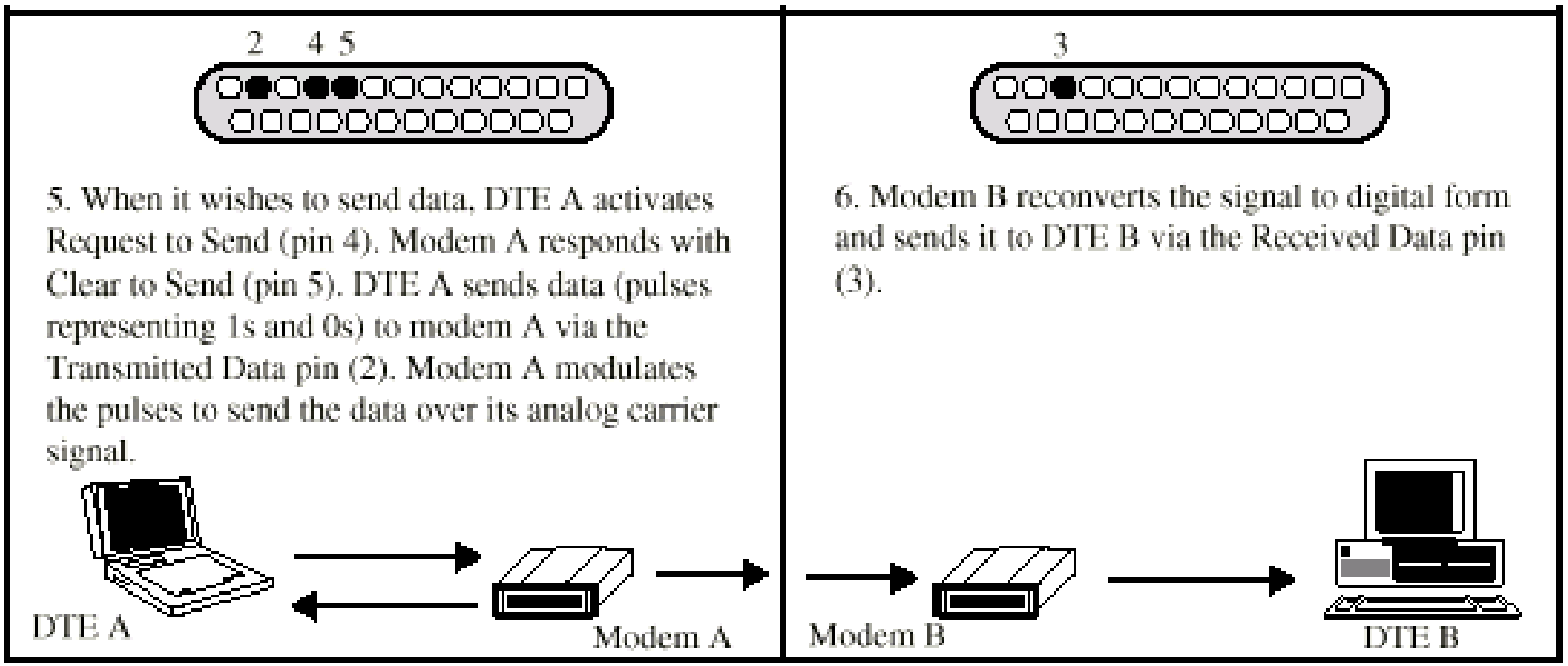
Dial Up Operation (1)



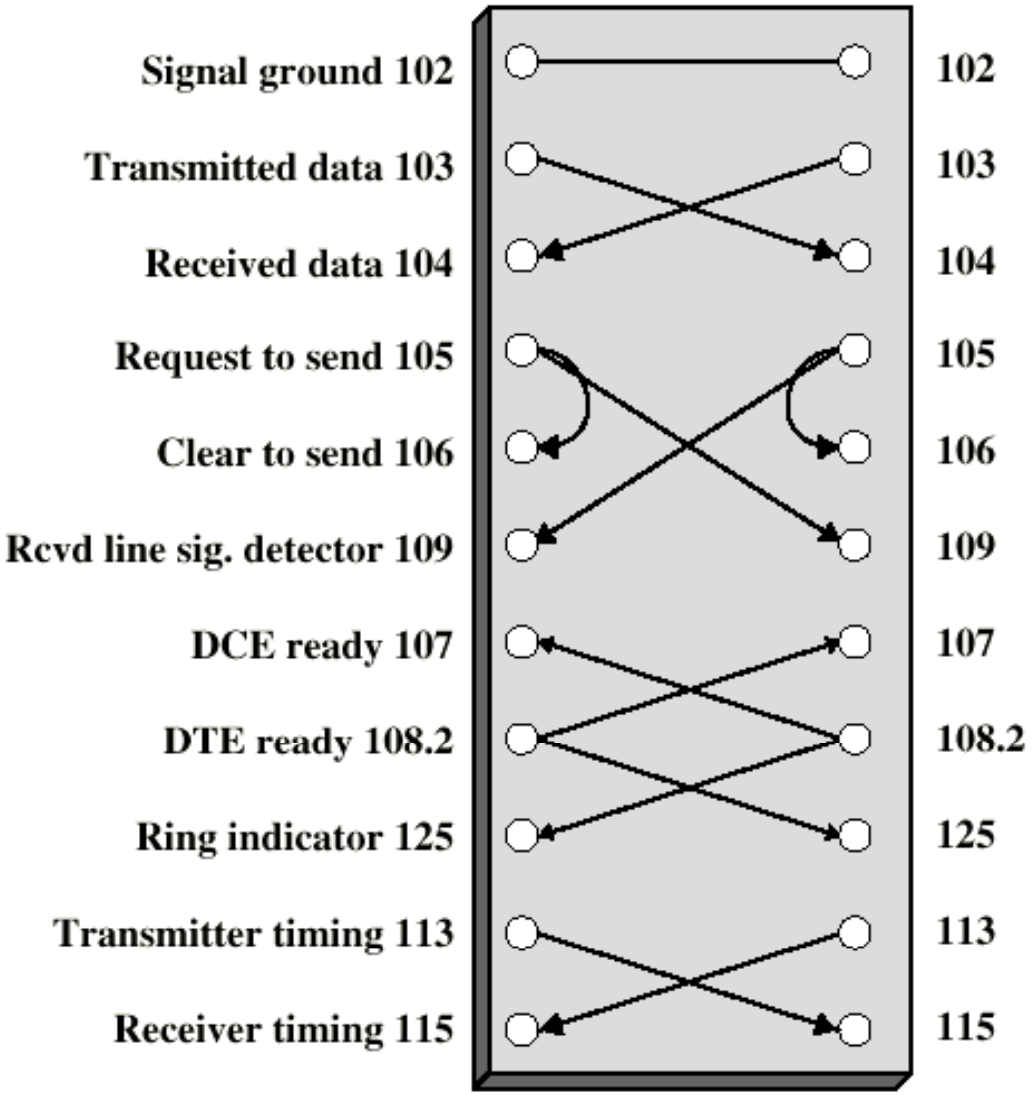
Dial Up Operation (2)



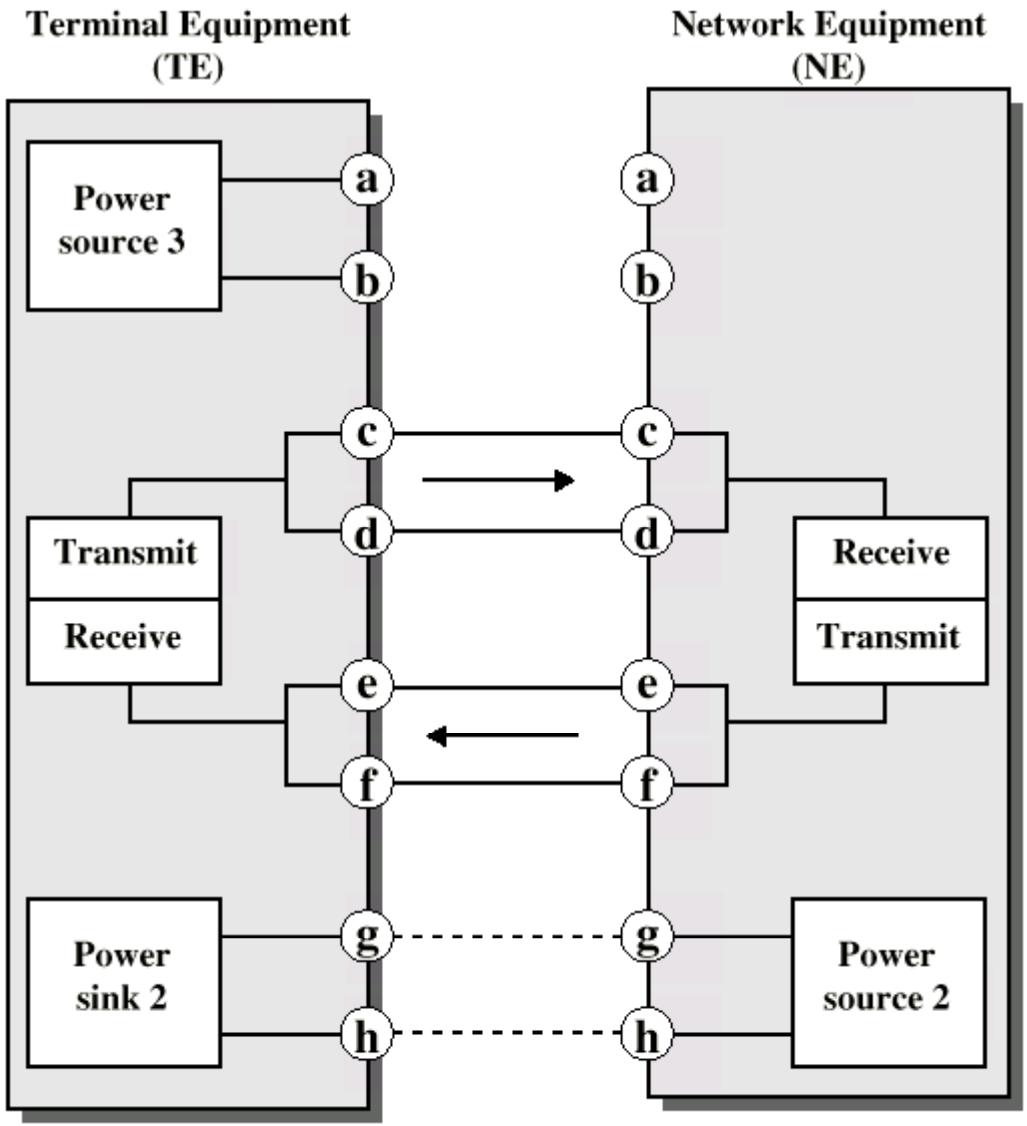
Dial Up Operation (3)



Null Modem


Signal ground 102
Transmitted data 103
Received data 104
Request to send 105
Clear to send 106
Rcvd line sig. detector 109
DCE ready 107
DTE ready 108.2
Ring indicator 125
Transmitter timing 113
Receiver timing 115
102
103
104
105
106
109
107
108.2
125
113
115

ISDN Physical Interface Diagram



ISDN Physical Interface

- Connection between terminal equipment (c.f. DTE) and network terminating equipment (c.f. DCE)
- ISO 8877
- Cables terminate in matching connectors with 8 contacts
- Transmit/receive carry both data and control

ISDN Electrical Specification

- Balanced transmission
  - Carried on two lines, e.g. twisted pair
  - Signals as currents down one conductor and up the other
  - Differential signaling
  - Value depends on direction of voltage
  - Tolerates more noise and generates less
  - (Unbalanced, e.g. RS-232 uses single signal line and ground)
  - Data encoding depends on data rate
  - Basic rate 192kbps uses pseudoternary
  - Primary rate uses alternative mark inversion (AMI) and B8ZS or HDB3